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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,061	12/11/2003	Wing K. Luk	YOR920030136US1 (8728-621)	1252
46/69 7590 02/20/2008 F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797				
EXAMINER				
BERNSTEIN, ALLISON				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/735,061

Applicant(s)

LUK ET AL.

Examiner

ALLISON P. BERNSTEIN

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33, 54, 55 and 58 is/are pending in the application.
- 4a) Of the above claim(s) 11-33, 54 and 55 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Acknowledgment is made of applicant's amendment, filed on 31 December 2007. The changes and remarks disclosed therein have been considered.

Claims 1-33, 54-55, and 58 are pending in the application. Claims 11-33 and 54-55 are withdrawn from further consideration. Claim 1 is currently amended. Claim 1 is the only independent claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 2, and 58** are rejected under 35 U.S.C. 102(b) as being anticipated by Houghton et al. (US 5,757,693) ("Houghton").

3. **Regarding claim 1**, Houghton discloses, in figure 1, a gated diode memory cell comprising: at least one transistor (for example Tw0) having a diffusion region and a gate connected directly to a write wordline (WLW0); and a gated diode (for example Tr0) having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline (for example WLR0).

4. **Regarding claim 2**, Houghton discloses, in figure 1, a gated diode memory cell as defined in Claim 1 wherein the first terminal of the gated diode (for example Tr0) forms one terminal of a storage cell and the second terminal of the gated diode (for example Tr0) forms another terminal of the storage cell.
5. **Regarding claim 58**, Houghton discloses, in figure 1, a gated diode memory cell as defined in claim 1 wherein the at least one transistor (for example Tw0) and gated diode (for example Tr0) are a same type of FET (see figure 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claims 3-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Houghton et al. (US 5,757,693) ("Houghton") in view of Hsu (US 2003/0147277).
8. **Regarding claim 3**, Houghton discloses a gated diode memory cell as defined in claim 2 wherein the first terminal is a gate of the gated diode.
9. Houghton does not disclose wherein the gate is implemented in the form of a shallow trench.
10. Hsu discloses in figures 4 and 9A-9D a gated diode memory cell wherein the gate (906A) is implemented in the form of a shallow trench (abstract and [0064]).

11. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device of Houghton with a gate that is implemented in the form of a shallow trench in view of the teachings of Hsu for the purpose of achieving significant area reduction ([0016] of Hsu).

12. **Regarding claim 4**, the Houghton/Hsu combination further discloses a gated diode memory cell as defined by claim 3, wherein the gate of the (for example 906A in figure 9D of Hsu) of the gated diode (for example 220 of Hsu) comprises a poly trench (906A in figure 9D of Hsu) surrounded by thin oxide (905B of Hsu) with silicon (for example 913 of Hsu) disposed underneath and surrounding the thin oxide (905B of Hsu) (see also [0069] of Hsu).

13. **Regarding claim 5**, the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 4 wherein the poly trench (906A of Hsu) is cylindrical (see figures 9A-9D of Hsu).

14. **Regarding claim 6**, the Houghton/Hsu combination further discloses a gated diode memory cell as defined in claim 4 wherein the gate (for example 906A in figure 9D of Hsu) of the gated diode (for example 220 of Hsu) comprises a metal oxide semiconductor ("MOS") capacitor ([0064] and [0033] of Hsu).

15. **Regarding claim 7**, Houghton discloses a gated diode memory cell as defined in Claim 2.

16. Houghton does not disclose wherein the gate of the gated diode is planar.

17. Hsu discloses in figures 4 and 3A-3B wherein the gate (216) of the gated diode (for example 220) is planar (see figure 3A).

18. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device of Houghton with a gate that is planar in view of the teachings of Hsu since planar gates are commonly used in the art.

19. **Regarding claim 8**, the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 7 wherein the gate (216 of Hsu) of the gated diode (for example 220 of Hsu) is disposed above a diffusion area (below 215 in figure 3A of Hsu).

20. **Regarding claim 9**, the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 8, further comprising an oxide layer (215 of Hsu) disposed between the gate (216 of Hsu) of the gated diode (220 of Hsu) and the diffusion area (below 215 of Hsu).

21. **Regarding claim 10**, the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 7, wherein the gated diode (220 of Hsu) comprises a planar metal oxide semiconductor ("MOS") capacitor([0033] of Hsu).

Response to Arguments

22. Applicant's arguments filed 31 December 2007 with respect to the Houghton reference have been fully considered but they are not persuasive.

23. Applicant argues that Tr0 of Houghton is not a diode.

24. In response every transistor comprises a diode and a gate; therefore every transistor comprises a gated diode. There is no claimed structure that distinguishes the claimed "gated diode" over Tr0 in Houghton.

25. Applicant's arguments, see page 7, filed 31 December 2007, with respect to Hsu have been fully considered and are persuasive. The 35 U.S.C. 102 rejections of claims 1-10 have been withdrawn.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLISON P. BERNSTEIN whose telephone number is

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(571)272-9011. The examiner can normally be reached on M-Tu 5:30am-5pm, W 5:30am-4pm, Th 5:30am-2pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

APB

/Richard Elms/
Supervisory Patent Examiner, Art Unit 2824
2.15.08